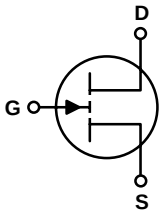
INN100EA035A

1. General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in En-FCLGA with 3.3 mm x 3.3 mm package size.

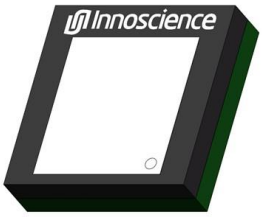


2. Features

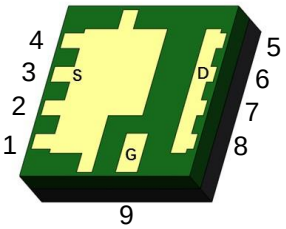
- GaN-on-Silicon E-mode HEMT technology
- Industry Application
- Very low gate charge
- Ultra-low on resistance
- Very small footprint

3. Applications

- High frequency DC-DC converter
- High density DC/DC power module
- Synchronous Rectification
- Motor driver
- Solar system MPPT



Top View



Bottom View

4. Key performance parameters

Table 1 Key performance parameters at T_J = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	3.5	mΩ
$Q_{G,typ}$ @ V_{DS} = 50V	7.6	nC
$I_{DS,Pulse}$(T_J = 25 °C)	230	A
Q_{OSS} @ V_{DS} = 50V	42	nC

5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
9	Gate	Driver Gate
1，2，3，4	Source	Source
5，6，7，8	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN100EA035A	En-FCLGA 3.3X3.3	J37

Table of contents

6. Maximum ratings

at T_J = 25 °C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage [1] (V_{GS} = 0 V, 1h total time, $T_A = T_{JMAX}$)	120	V
I_D	Continuous current (V_{GS} = 5 V, T_C=25 ˚C, $R_{\theta JC}$ = 0.49 ˚C/W)	201	A
	Continuous current (V_{GS} = 5 V, T_C=100 ˚C, $R_{\theta JC}$ = 0.49 ˚C/W)	127	A
	Continuous current (V_{GS} = 5 V, T_A=25 ˚C, $R_{\theta JA}$ = 62.41 ˚C/W)	17.8	A
	Pulsed (T_J=25˚C, T_{Pulse} = 300 µs)	230	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

Note:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation;

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.49	˚C/W	-
$R_{\theta JB}$	Thermal Resistance, Junction to Board	4.16	˚C/W	-
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [2]	62.41	˚C/W	-
	Thermal Resistance, Junction to Ambient [3], without heat sink	33.61	˚C/W	-
	Thermal Resistance, Junction to Ambient [4], with 12.25cm^2 heat sink	26.22	˚C/W	-
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note:

2. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
3. Device on 60mm*36mm*1.6mm PCB FR4 with four layers, 2 oz copper.
4. Device on 60mm*36mm*1.6mm PCB FR4 with four layers, 2 oz copper. The heat sink (35mm*35mm*15mm) is vertically placed on the top of the device.

8. Electric characteristics

at T_J = 25 °C, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{DSS}	Drain Source Leakage	-	1	100	μA	V_{GS} = 0 V, V_{DS} = 100 V
I_{GSS}	Gate-to-Source Forward Leakage	-	0.5	100	μA	V_{GS} = 6 V
	Gate-to-Source Reverse Leakage	-	0.1	100	μA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.1	V	V_{DS} = V_{GS}, I_D = 7.6 mA
$R_{DS(on)}$	Drain-Source On-state Resistance [5]	-	2.9	3.5	mΩ	V_{GS} = 5 V, I_D = 25 A
V_{SD}	Source-Drain Forward Voltage	-	1.5	-	V	I_S = 5 A,V_{GS} = 0 V

Note:

5. $R_{DS(on)}$ is measured without prior drain bias or switching stress.

Table 7 Dynamic characteristics [6]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	905	-	pF	V_{GS} = 0 V, V_{DS} = 50 V
C_{OSS}	Output Capacitance	-	425	-		V_{GS} = 0 V, V_{DS} = 50 V
C_{RSS}	Reverse Transfer Capacitance	-	7	-		V_{GS} = 0 V, V_{DS} = 50 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	595	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	835	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
R_G	Gate resistance	-	1.5	-	Ω	f = 5MHz, open drain
Q_G	Total Gate Charge	-	7.6	-	nC	V_{GS} = 5 V, V_{DS} = 50 V, I_D = 25 A
Q_{GS}	Gate to Source Charge	-	1.6	-		V_{DS} = 50 V, I_D = 25 A
Q_{GD}	Gate to Drain Charge	-	1.5	-		V_{DS} = 50 V, I_D = 25 A
$Q_{G(TH)}$	Gate Charge at Threshold	-	0.9	-		V_{DS} = 50 V, I_D = 25 A
Q_{OSS}	Output Charge	-	42	-		V_{GS} = 0 V, V_{DS} = 50V
Q_{rr}	Reverse recovery charge	-	0	-		V_{DS} = 50 V, I_S = 25 A

Note:

6. Guaranteed by design.

9. Electric characteristics diagrams

at T_J = 25 °C, unless specified otherwise

Fig. 1 Typical Output Characteristics (T_J=25°C)

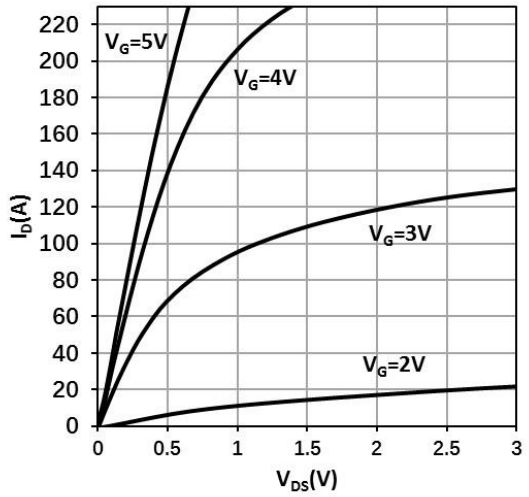


Fig. 2 Typical Output Characteristics (T_J=125°C)

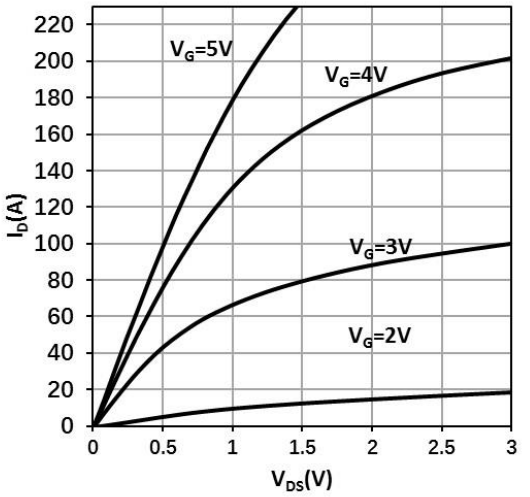


Fig.3 Typical Drain On-state Resistance (T_J=25°C)

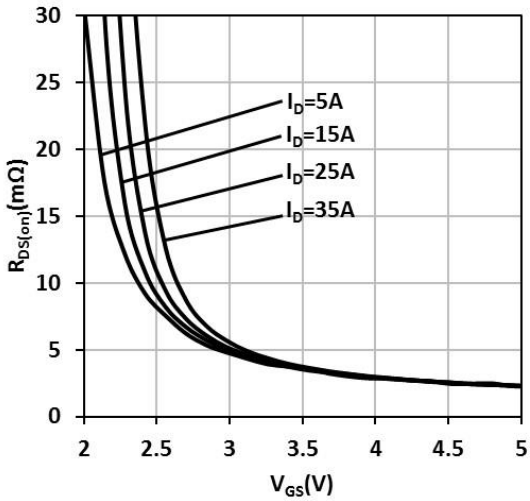


Fig. 4 Typical Drain On-state Resistance (T_J=125°C)

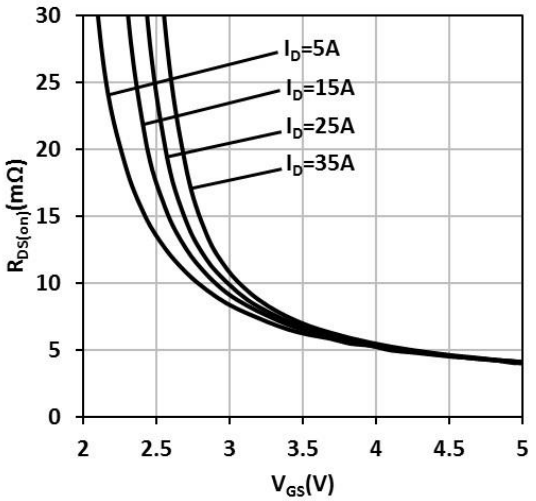


Fig. 5 Normalized On-State Resistance vs. Temp.

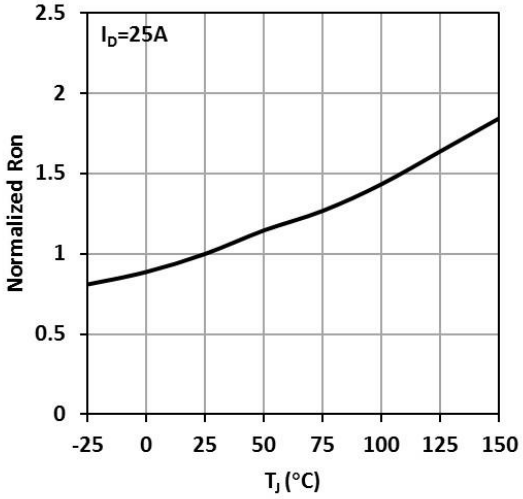


Fig. 6 Typical Transfer Characteristics

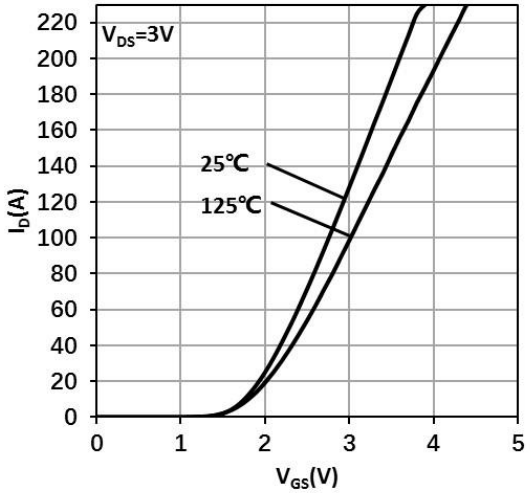


Fig. 7 Typ. Reverse Drain-Source Characteristics (V_{GS}≤0,T_J =25°C)

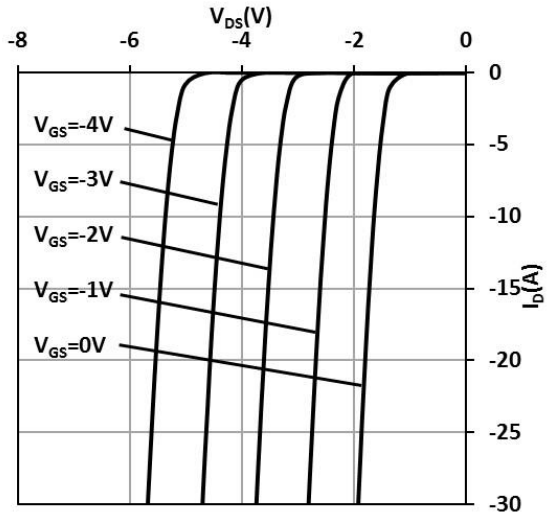


Fig. 8 Typ. Reverse Drain-Source Characteristics (V_{GS}≥0,T_J =25°C)

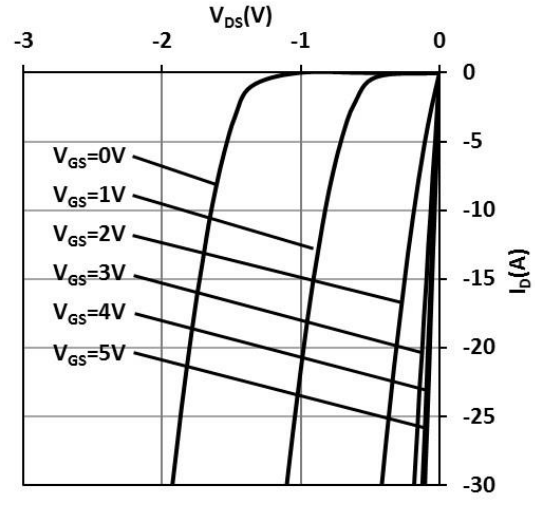


Fig. 9 Typ. Reverse Drain-Source Characteristics (V_{GS}≤0, T_J = 125°C)

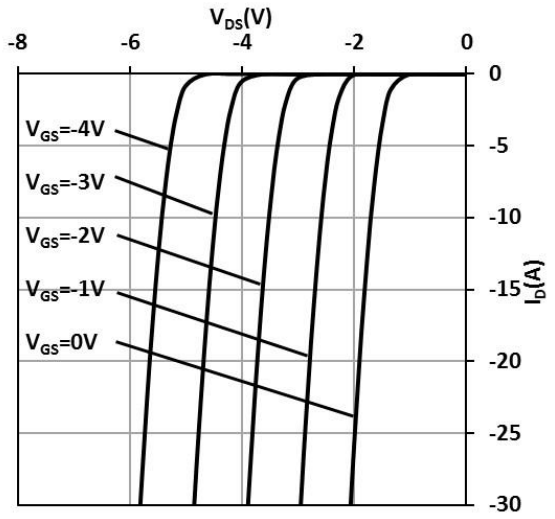


Fig. 10 Typ. Reverse Drain-Source Characteristics (V_{GS}≥0,T_J = 125°C)

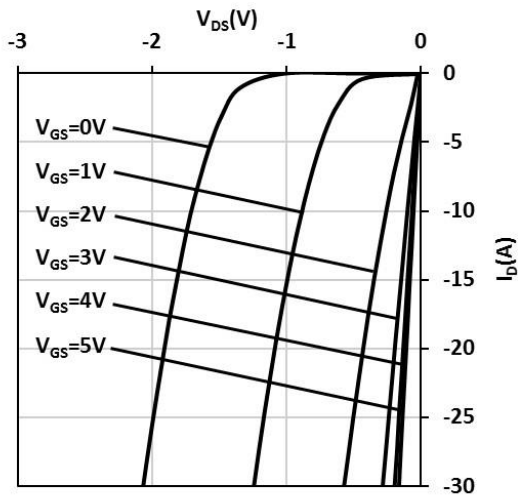


Fig. 11 Typ. Capacitances Characteristics

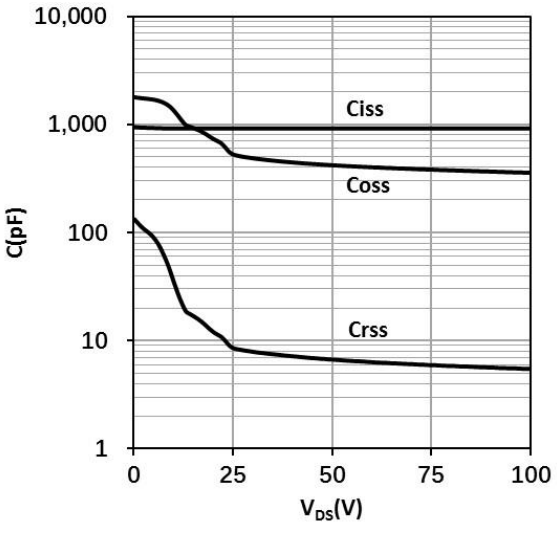


Fig. 12 Typ. Gate Charge

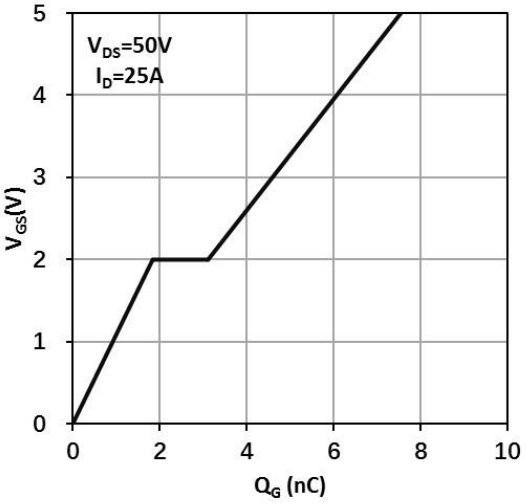


Fig. 13 Normalized Threshold Voltage vs. Temp.

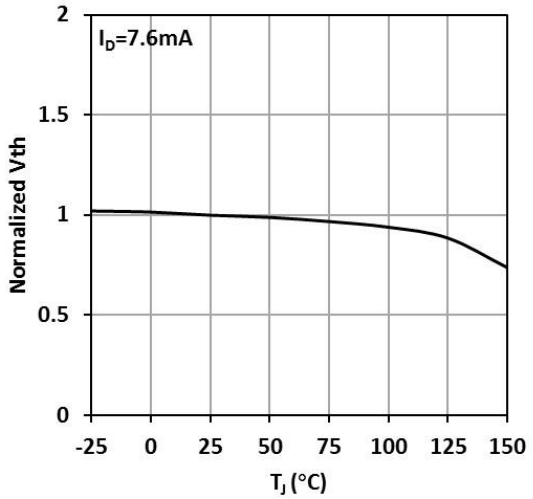


Fig. 14 Output Charge

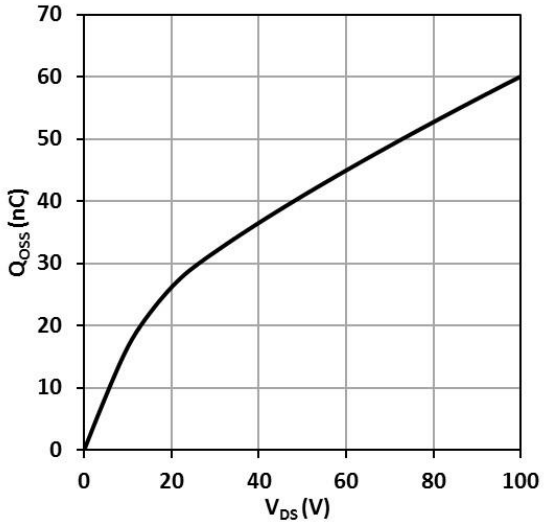


Fig. 15 Output Capacitance Stored Energy

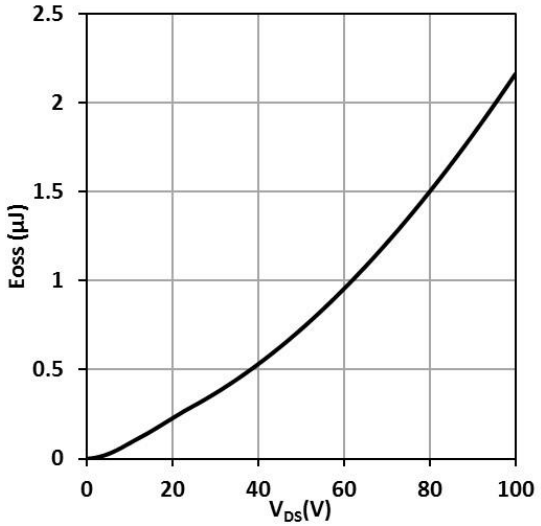


Fig. 16 Power Dissipation

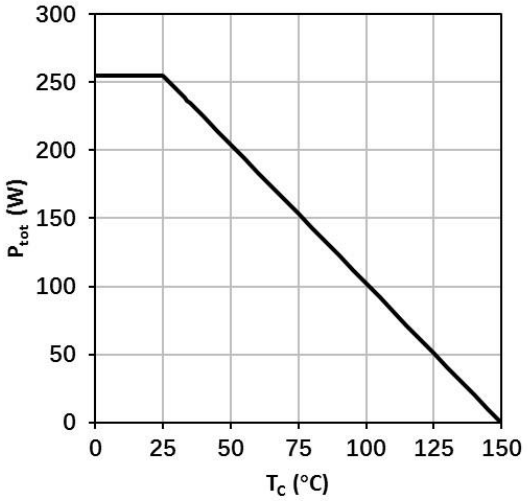


Fig. 17 Safe Operating Area
$I_D=f(V_{DS})$; $T_C=25°C$; single pulse; parameter:t_p

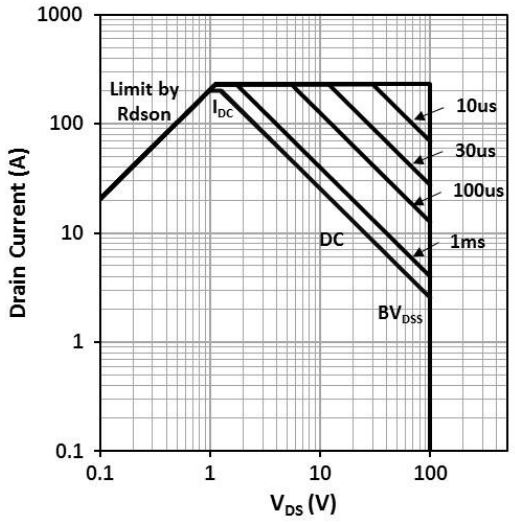
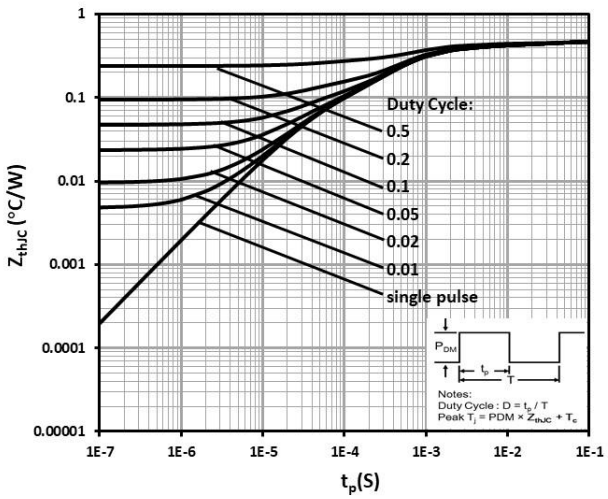
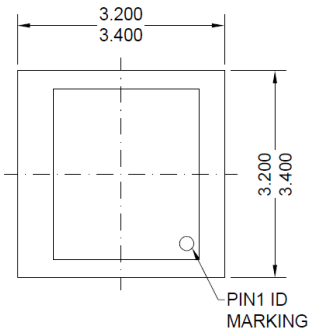


Fig. 18 Max. Transient Thermal Impedance
$Z_{thJC}=f(t_p)$; parameter:$D=t_p/T$

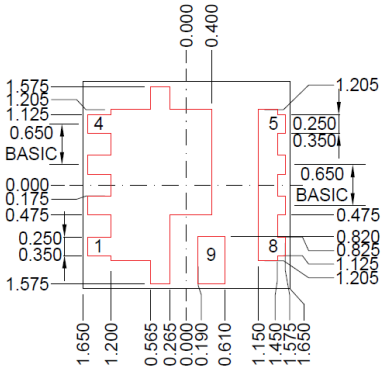


10. Package outlines

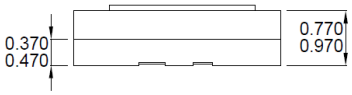
Package Reference



TOP VIEW



BOTTOM VIEW

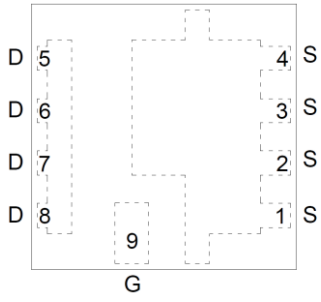


SIDE VIEW

NOTE:

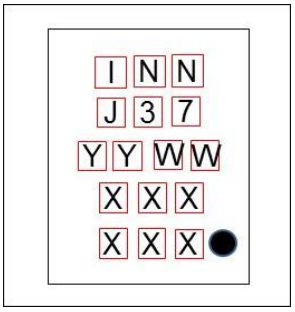
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

PIN configuration



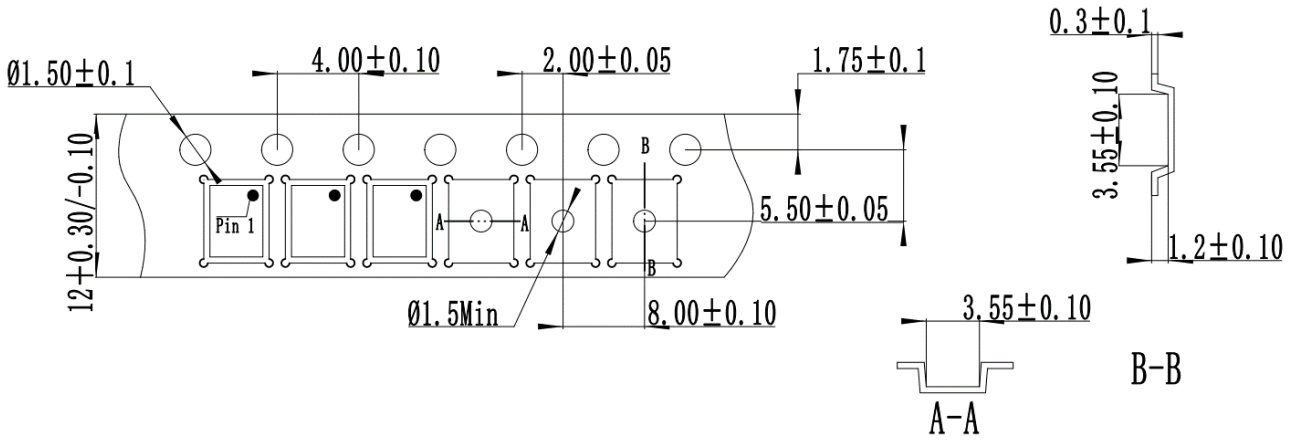
Top View

Marking Reference

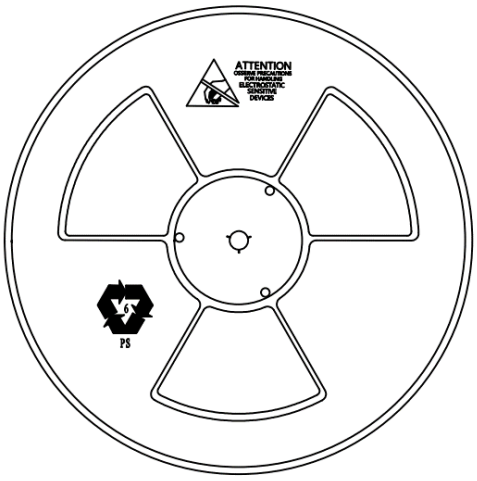


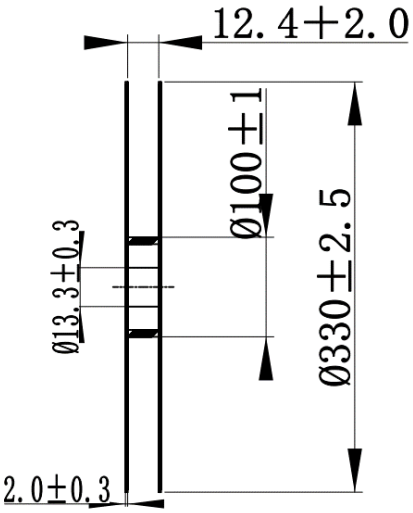
Row	Description	Example
Row 1	Company Name	INN
Row 2	Product Code	J37
Row 3	Date code	YYWW
Row 4	Lot code	XXX
Row 5		XXX

11. Reel information



Notes:
(1)The cumulative error of any 10 sprocket holes shall not exceed ± 0.20mm;
(2)The material thickness shall be measured based on the edge of the carrier tape;
(3)The unspecified tolerance is ± 0.1mm, and R<0.3mm is not specified;
(4)The unmarked demolding slope is 5 ° ;
(5)Surface Resistivity: 1*10 e 5 Ω/Δ~ 1*11 e11

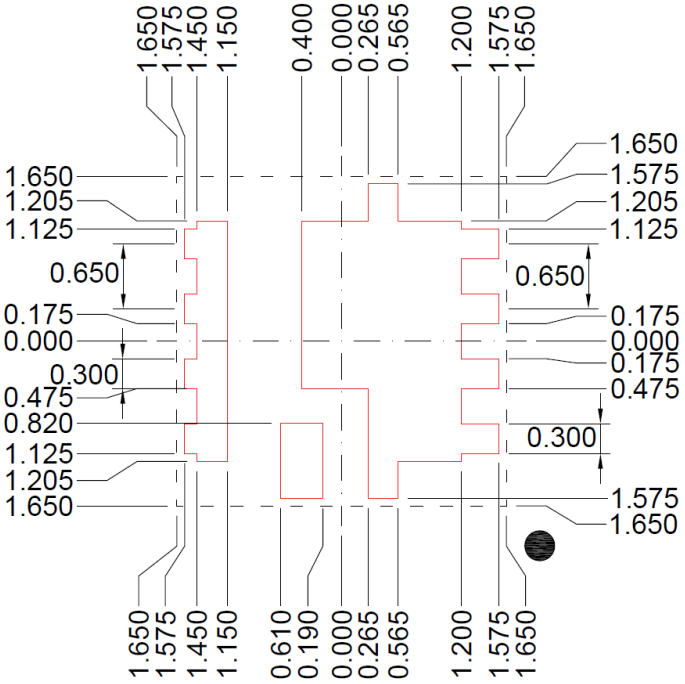




Notes:
1、The surface of the product should be smooth, clean, and free of injection molding defects, and there should be no significant burrs;
2、Material surface resistance:1*10e5Ω/Δ~1*10e10Ω/Δ;
3、No tolerance marked: ±0.3mm;

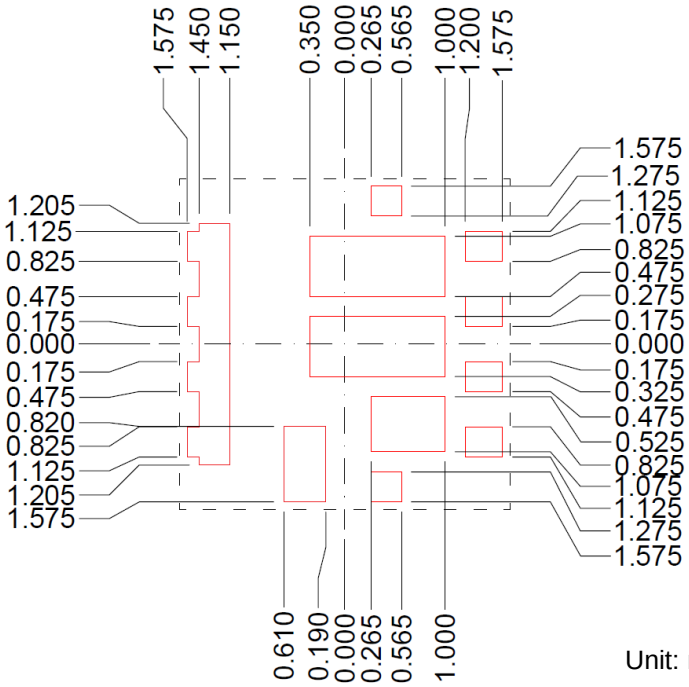
12. Land Pattern

Recommended land pattern



Unit: mm

Recommended Stencil drawing



Unit: mm

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-12-26	1.0 Version release.

Important Notice

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